Low-voltage Organic Field-effect Transistors with a Gate Insulator of Ta₂O₅ Formed by Sputtering

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The Ta₂O₅ film prepared on silicon by RF sputtering has been used as a gate insulator for the top-contact field-effect transistors fabricated with poly(2-methoxy-5-(2'-ethylhexyloxy)-1,4-phenylenevinylene) (MEH-PPV) or pentacene. Good transistor characteristics have been obtained with saturation at low drive voltages (about -3 V) and with hole mobilities of 5.2×10^{-4} cm²/Vs (MEH-PPV) and 0.8 cm²/Vs (pentacene).

Organic field-effect transistors (OFETs) have recently received increasing interest because of their potential applications including flat-panel displays, IC tags, and smart cards.^{1,2} Important parameters characterizing OFETs are carrier mobility, on/ off current ratio, and drive voltage. Silicon dioxide thermally grown on heavily doped Si is commonly used as the gate insulator material of OFETs. Most of the OFETs with SiO₂ operate at a few tens of volts, which exceed drive voltages for many applications. One of promising ways to enable device operation at low drive voltages is to use an insulator with high dielectric constant such as barium zirconate titanate $(\mathcal{E}_r, 17)$,³ tantalum oxide $(\mathcal{E}_r,$ 20–23),⁴⁻⁶ titanium oxide (\mathcal{E}_r , 41),⁷ and aluminum oxide (\mathcal{E}_r , 10) instead of SiO₂ (\mathcal{E}_r , 3.9). Tantalum oxide layers have been made by anodization,^{4,6} electron-beam evaporation,⁵ sputtering,⁸ and low-pressure chemical vapor deposition.9 In this work, we report the performance of organic field-effect transistors with a tantalum oxide layer formed by RF sputtering as a gate insulator.

Top-contact OFETs were fabricated on a doped n⁺-Si(100) plate, as shown in Figure 1. A SiO₂ layer on the doped Si substrate was removed with a 5% aq. solution of HF. A film of Ta₂O₅ was formed onto this Si surface by RF sputtering with an ANELVA SPF-332H apparatus. Sputtering was performed from a Ta₂O₅ target (99.99%, Toshima Seisakujo) in the atmosphere of Ar, O₂, and Ar–O₂ mixtures (50 and 20% O₂ contents)



Leak currents measured for the Ta_2O_5 film (260-nm thickness) formed in the atmosphere of 80% Ar and 20% O₂ are plotted with closed circles in Figure 2. The applied electric field ranges from -0.3 and 0.3 MV/cm, corresponding to about -8 and 8 V, respectively. The Ta_2O_5 film shows low leak currents in the whole range of the applied voltages, while leakage is observed for the film prepared in Ar (open circles). Kozawaguchi et al.⁸ showed that the RF sputtering in an atmosphere of 80% Ar and 20% O₂ suppresses the formation of oxygen defects which become electron traps. The Ta_2O_5 films prepared in the atmosphere of O₂ and Ar (50%)–O₂ (50%) mixture have been easily



Figure 1. Schematic structure of an organic field-effect transistor based on Ta_2O_5 as a gate insulator.



Figure 2. Leak currents for the Ta_2O_5 films formed by sputtering in the atmosphere of Ar (\bigcirc) and 80% Ar–20% O_2 mixture (\bullet).

destroyed by the application of a voltage. The observed images of SEM and AFM show that the surface of the Ta_2O_5 layer is very smooth and uniform. The root-mean-square roughness of the surface in the AFM image is 0.045 nm. These results indicate that the Ta_2O_5 films formed by sputtering in the atmosphere of 80% Ar and 20% O_2 are suitable for use as the insulator layer of OFETs.

Figure 3 plots the I_D versus V_D characteristics for an FET based on MEH-PPV. When the gate electrode is biased negatively with respect to the source electrode, the FET operates in the accumulation mode and the accumulated charges are holes. The observed results indicate that MEH-PPV behaves as a p-type semiconductor. No n-type behaviors are observed for positive gate voltages. Saturation behaviors in the drain current are observed at very low voltages of -3 V. Iino et al.⁶ reported that the FET based on Ta₂O₅ formed by anodization of Ta shows the best performance at an operating voltage of -5 V. The hole mobility μ_h has been calculated form the observed saturation current $I_{D, sat}$ by using the following equation:¹⁰

$$I_{\rm D, \ sat} = \frac{WC\mu_{\rm h}}{2L} (V_{\rm G} - V_{\rm T})^2 \tag{1}$$

where $V_{\rm T}$ is the threshold voltage; *C* is the capacitance per unit area of the gate insulator; the capacitance is 163 nF/cm². From the least-square fitting, the hole mobility in MEH-PPV is found to be $5.2 \times 10^{-4} \text{ cm}^2/\text{Vs}$ and the threshold voltage -0.8 V. The on/off current ratio is defined as the ratio of the drain currents between the on state ($V_{\rm G}$, -3 V) and the off state ($V_{\rm G}$, 0 V) at the drain-to-source voltage of -4 V. The observed on/off ratio is 1500.



Figure 3. Plot of drain current (I_D) versus drain-to-source voltage (V_D) for various gate voltages from an MEH-PPV FET with Ta₂O₅ as a gate insulator.

Figure 4 shows the I_D-V_D characteristics for a pentacene FET. The observed result means that pentacene behaves as a p-type semiconductor. No n-type behaviors are observed for positive gate voltages. Saturation behaviors in the drain current are observed. From the observed drain currents in the saturation regime, the hole mobility in pentacene is calculated to be $0.8 \text{ cm}^2/\text{Vs}$ and the threshold voltage -0.3 V. The obtained field-effect mobility is similar to those reported in the literature (0.6– $2.4 \text{ cm}^2/\text{Vs}$).² The on/off current ratio means the ratio of the

drain currents between the gate voltages of -2 and 0 V at the drain-to-source voltage of -3 V. The observed ratio is 66. The observed on/off ratio is much smaller than that for the MEH-PPV FET. Probably, this result originates from the low purity of pentacene. It should be noted that the primary goal here is to examine the operating voltages of OFETs with Ta₂O₅ as a gate insulator.



Figure 4. Plot of drain current (I_D) versus drain-to-source voltage (V_D) for various gate voltages from a pentacene FET with Ta₂O₅ as a gate insulator.

In summary, it has been demonstrated that the OFETs with Ta_2O_5 prepared by RF sputtering as gate insulator material operate at low gate voltages of about -3 V.

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